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ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/707,296	YANG, HO-HSING	
	Examiner	Art Unit	
	William L. Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, November 5th, 2007, the Applicant amended claims 1-5, 7-9, 11-12, 14-18, 21-23, 25-27 and 29. Currently claims 1-30 are pending.

Drawings

2. The drawings were received on November 5th, 2007. These drawings are acceptable.

Response to Arguments

3. Applicant's arguments filed November 5th, 2007 have been fully considered but they are not persuasive.

4. On page 37 of the Remarks, the Applicant argues that Lie's second frame data does not correspond with the present invention as set forth in claim 7.

The Examiner respectfully disagrees. The phrasing pointed out by the Applicant only requires that the signal converter operate "in response to said second frame data and said second third frame data." From figure 4, it is apparent that where the second frame data not present that the motion estimator would not function. Therefore the signal converter of Lei operates in response to the second and third frame data. Furthermore it is important to point out that the data compared by the signal converter is delayed frame data output from the frame memory and data that is identical to the second frame data that is input to the frame memory.

5. On pages 39-40, the Applicant traverses the rejection of claim 15, stating that neither Lei nor Van Asma disclose a first-fifth frame data. Additionally, the Applicant

argues that the line memory of Van Asma does not meet the technical limitations required of claim 15.

The Examiner must respectfully disagree. The rejection of claims 15-20 have been expanded upon to hopefully further illustrate how the combination of Van Asma and Lei read on claims 15-20.

As to the line memory of Van Asma, the Examiner must once again disagree. Claim 15 does not require that the signal converter have multiple output terminals or that the output be done simultaneously. All that claim 15 requires is that a "fourth frame data and a fifth frame data" be output. Van Asma's line memory and Lei's generator both disclose this limitation in their sequential output of frame data.

6. On pages 41-42 the Applicant argues that Lei does not disclose the majority of frame memories claimed in claim 21. Applicant additionally argues that the first data flow switcher limitations are more technically substantial than the line memory of Van Asma.

As to the seeming overlap in labeled frame data in the rejection of claim 21, their is no claim language requiring that the two different data flows happen simultaneously or occur through different terminals. As such the circuitry of the combination between Lei and Van Asma discloses the claim in the sense that the new data continually flows into the device and each new frame data is newly numbered. Therefore the first output of 72 in Lei is seen as the second frame data, and the subsequent output of 72 is seen as the fourth frame data.

Additional arguments regarding the technical feasibility of the line memory of Van Asma have been addressed in above arguments.

7. As shown above the rejections are seen as proper and are thus maintained.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-6, 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, claim 1 states that the first and second frame data are compared. In direct contrast to this claim 4 states that the fourth and fifth frame data are compared. This clear disparity causes claims 1-6 to be indefinite.

Claims 15-17 also directly contradict one another. For example, claim 15 states that the first data flow switcher, "outputs one of said first frame data and third frame data." Claim 16, however, directly contradicts this stating that the first data flow switcher outputs "one of said third frame data and said tenth frame data." A similar contradiction occurs with respect to the second data flow switcher and claims 15 and 17.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Lei (US 6,130,911).

With respect to claim 7, Lei discloses, a circuit for enhancing motion picture quality, comprising:

a nonlinear quantizer (72 in fig. 4) receiving a first frame data (input of 72) and quantizing said first frame data by using a nonlinear quantization method to output a second frame data (output of 72);

a frame memory module (100 in fig. 4), coupled to said nonlinear quantizer, for receiving said second frame data (input of 100) and outputting a third frame data (output of 100) corresponding to said second frame data, said second frame data being shown in a motion picture after said third frame data (clear from fig. 4); and

a signal-converter (70, 80 in fig. 4), in response to said second frame data (input into 100) and said third frame data (output of 100) corresponding to said second frame data, for obtaining a compensation data (output of 80) to compensate said first frame data for outputting a fourth frame data (output of 70 in fig. 4).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-6 and 8-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lei (US 6,130,911) in view of Van Asma (US 6,489,964).

With respect to claim 1, Lei discloses, a circuit for enhancing motion picture quality (fig. 4), comprising:

a frame memory, for storing a motion picture data (78 in fig. 4);

a signal-converter (70, 80 in fig. 4), for receiving a first frame data and a second frame data (fig. 1) and comparing said first frame data and said second frame data (col. 1, lines 50-54; col. 6, lines 33-34) to generate a compensation data and output a third frame data (output of 70 in fig. 4).

Lei does not expressly disclose, including buffers and a multiplexer in the circuit.

Van Asma discloses, a circuit for simplifying display circuitry, comprising:

a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a first frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said first frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO2), and first-in-first-out outputting said second frame data (output of FIFO2); said first frame data being shown in a motion picture after said second frame data (clear from fig. 3);

a frame memory, for storing a motion picture data (SDRAM in fig. 3);

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of

said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace small frame memory of Lei with the frame buffer, containing a multiplexer unit, of Van Asma.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

With respect to claim 2, Lei and Van Asma disclose, the circuit of claim 1 (see above).

Lei further discloses, a first data latch (76 in fig. 4), for receiving a fourth frame data (input of 76) and outputting said first frame data, the number of bits of said first frame data is larger than the number of bits of said fourth frame data (col. 4, lines 55-61, for example);

a second data latch (82 in fig. 4), for receiving a second frame data (input of 82) and outputting a fifth frame data, the number of bits of said second frame data is larger than the number of bits of said fifth frame data (col. 6, line 45 for example);

wherein said signal-converter (70 in fig. 4) is for obtaining said compensation data to output said third frame data in response to said fourth frame data and said fifth frame data corresponding to said second frame data (clear from fig. 4).

With respect to claim 3, Lei and Van Asma disclose, the circuit of claim 2 (see above).

Lei further discloses, a nonlinear quantizer (72 in fig. 4) receiving a sixth frame data (input of 72 in fig. 4) and quantizing said sixth frame data by using a nonlinear quantization method to output said fourth frame data (output of 72; input of 76), said signal-converter receiving said sixth frame data (input of 70 in fig. 4) and compensating said sixth frame data based on said compensation data to obtain said third frame data (clear from fig. 4).

With respect to claim 4, Lei and Van Asma disclose, the circuit of claim 3 (see above).

Lei further discloses, a motion picture enhancing unit (80 in fig. 4), for simultaneously receiving said fourth frame data and said fifth frame data and comparing said fourth frame data and said fifth frame data to generate said compensation data based on the difference between said fourth frame data and said fifth frame data (col. 1, lines 50-54; col. 6, lines 33-34); and

a data processing unit (70 in fig. 4), for simultaneously receiving said sixth frame data and said compensation data corresponding to said sixth frame data, and compensating said sixth frame data based on said compensation data to obtain said third frame data (col. 6, lines 50-52).

With respect to claim 5, Lei and Van Asma disclose, the circuit of claim 2 (see above).

Lei further discloses, wherein the number of bits of said first frame data are integral of the number of bits of said fourth frame data, and the number of bits of said second frame data is said integral of the number of bits of said fifth frame data (col. 7, lines 57-59).

With respect to claim 6, Lei and Van Asma disclose, the circuit of claim 1 (see above).

Lei does not expressly disclose, wherein said circuit is applied to a liquid crystal display.

Van Asma further discloses, wherein said circuit is applied to a liquid crystal display (col. 4, lines 53-56).

It would have been obvious to one of ordinary skill in the art to use the circuit of Lei in a liquid crystal display as taught by Asma, due to the well-known slow response of liquid crystal displays which makes them especially susceptible to motion artifacts.

With respect to claim 8, Lei discloses, the circuit of claim 7 (see above), wherein said frame memory module comprises:

a frame memory (78 in fig. 4).

Lei does not expressly disclose including buffers and a multiplexer in the frame memory module.

Van Asma discloses, a circuit for simplifying display circuitry, comprising:

a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said second frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a third frame data (input of FIFO2), and first-in-first-out outputting said third frame data (output of FIFO2);

a frame memory, for storing a motion picture data (SDRAM in fig. 3); and

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory,

for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said third frame data from said frame memory to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace small frame memory of Lei with the frame buffer, containing a multiplexer unit, of Van Asma.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

With respect to claim 9, Lei and Van Asma disclose, the circuit of claim 8 (see above).

Lei further discloses, a motion picture enhancing unit (80 in fig. 4), for simultaneously receiving said third frame data (right input of 80 in fig. 4) and said second frame data (top input in fig. 4; data here is identical to data input to 100) and comparing said second frame data and said third frame data to generate said compensation data based on the difference between said second frame data and said third frame data (col. 1, lines 50-54; col. 6, lines 33-34); and

a data processing unit (70 in fig. 4), for simultaneously receiving said first frame data and said compensation data corresponding to said first frame data, and compensating said first frame data based on said compensation data to obtain said fourth frame data (col. 6, lines 50-52).

With respect to claim 10, Lei and Van Asma disclose, the circuit of claim 8 (see above).

Lei does not expressly disclose, wherein said circuit is applied to a liquid crystal display.

Van Asma further discloses, wherein said circuit is applied to a liquid crystal display (col. 4, lines 53-56).

It would have been obvious to one of ordinary skill in the art to use the circuit of Lei in a liquid crystal display as taught by Asma, due to the well-known slow response of liquid crystal displays which makes them especially susceptible to motion artifacts.

With respect to claims 11-14, Lei and Asma disclose, the circuit of claims 1-4 (see above). As claims 11-14 are merely method versions of these claims, they are rejected on the same merits shown above in the rejections of claims 1-4.

With respect to claim 15, Lei discloses, a circuit for enhancing motion picture quality (fig. 4), comprising:

a frame memory, for storing a motion picture data (78 in fig. 4);

a signal-converter (70, 80 in fig. 4), for receiving a first frame data (output of 68 in fig. 4), a second frame data (output of 100 in fig. 4) and a third frame data (top input of 80 in fig. 4) to generate a compensation data and to output a fourth frame data (first output of 70) and a fifth frame data (subsequent output of 70);.

Lei does not expressly disclose, including buffers, data flow switchers and a multiplexer in the circuit.

Van Asma discloses, a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a first frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said first frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO2), and first-in-first-out outputting said second frame data (output of FIFO2); said first frame data being shown in a motion picture after said second frame data (clear from fig. 3);

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said

second frame data from said frame memory to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required); and

a first data flow switcher (input line memory in fig. 4), for receiving a sixth frame data (first input into "lin mem" in fig. 4) and a seventh frame data (subsequent input into "lin mem" in fig. 4) and transforming said sixth frame data and seventh frame data to output a first frame data and a third frame data, said first data flow switcher outputs one of said first frame data and said third frame data; and (sequential outputs of "lin mem" in fig. 4); and

a second data flow switcher (DA in fig. 4), for receiving said fourth frame data and said fifth frame data and transforming said fourth frame data and fifth frame data to output an eighth frame data and a ninth frame data, said second data flow switcher outputs one of said eighth frame data and said ninth frame data (sequential outputs of DA in fig. 4).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace small frame memory of Lei with the frame buffer of Van Asma and include the frame buffers, containing a multiplexer unit, and data flow switchers of Van Asma.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

With respect to claim 16, Lei and Van Asma disclose, the circuit of claim 15 (see above).

Lei, when combined with Van Asma as shown above, further discloses, a first data latch (Lei; 76 in fig. 4), coupled to and between said first data flow switcher and said first dual-port buffer, said first data flow is changed for receiving said sixth frame data and seventh frame data, and transforming said sixth frame data and said seventh frame data to output a tenth frame data and the third frame data, said first data flow switcher outputs one of said third frame data and said tenth frame data (Van Asma; inp lin mem in fig. 3), said first data latch, for receiving said tenth frame data (Lei; input of 76) and outputting said first frame data, the number of bits of said first frame data is larger than the number of bits of said tenth frame data (Lei; col. 4, lines 55-61, for example);

a second data latch (Lei; 82 in fig. 4), coupled to and between said first dual-port buffer and said signal-converter, for receiving said second frame data (Lei; input of 82) and outputting an eleventh frame data, the number of bits of said second frame data is larger than the number of bits of said eleventh frame data (Lei; col. 6, line 45 for example);

wherein said signal-converter (Lei; 70 in fig. 4), in response to said tenth frame data, said third frame data and said eleventh frame data corresponding to said third frame data obtains said compensation data to output said fourth frame data and said fifth frame data (Lei; clear from fig. 4).

With respect to claim 17, Lei and Van Asma disclose, the circuit of claim 16 (see above).

Lei, when combined with Van Asma as shown above, further discloses a first nonlinear quantizer (Lei; 72 in fig. 4), coupled to and between said first data flow switcher and said first data latch, said first data flow switcher is changed for receiving said sixth frame data and seventh frame data, and transforming said sixth frame data and said seventh frame data to output a twelfth frame data and the third frame data, said first data flow switcher outputs one of said third frame data and said twelfth frame data (Van Asma; DA in fig. 3), said first nonlinear quantizer receiving said twelfth frame data (Lei; input of 72 in fig. 4) and quantizing said twelfth frame data by using a nonlinear quantization method to output said tenth frame data (Lei; output of 72; input of 76); and

a second nonlinear quantizer (Lei; 66 in fig. 4), coupled to and between said first data flow switcher and said signal converter, for receiving said third frame data (Lei; input of 72 in fig. 4) and quantizing said third frame data by using a nonlinear quantization method to output said thirteenth frame data (Lei; output of 72; input of 76);

wherein said signal converter, in response to said twelfth frame data, said third frame data, and said thirteenth frame data corresponding to said eleventh frame data (Lei; input of 70 in fig. 4) obtains said compensation data to output said fourth frame data and said fifth frame data (Lei; clear from fig. 4).

With respect to claim 18, Lei and Van Asma disclose, the circuit of claim 17 (see above).

Lei further discloses, that the signal-converter comprises a motion picture enhancing unit (80 in fig. 4), for simultaneously receiving said thirteenth frame data and said eleventh frame data and comparing said thirteenth frame data and said eleventh frame data to generate said compensation data based on the difference between said thirteenth frame data and said eleventh frame data (col. 1, lines 50-54; col. 6, lines 33-34); and

a first data processing unit (70 in fig. 4), for simultaneously receiving said twelfth frame data and said compensation data corresponding to said twelfth frame data, and compensating said twelfth frame data based on said compensation data to obtain said fourth frame data (col. 6, lines 50-52)

a second data processing unit (68 in fig. 4), for simultaneously receiving said third frame data and said compensation data corresponding to said third frame data, and compensating said third frame data based on said compensation data to obtain said fifth frame data (col. 6, lines 50-52).

With respect to claim 19, Lie and Van Asma disclose, the circuit of claim 16 (see above).

Lei further discloses, wherein the number of bits of said first frame data are integral of the number of bits of said tenth frame data, and the number of bits of said second frame data are said integral of the number of bits of said eleventh frame data (col. 7, lines 57-59).

With respect to claim 20, Lei and Van Asma disclose, the circuit of claim 15 (see above).

Lei does not expressly disclose, wherein said circuit is applied to a liquid crystal display.

Van Asma further discloses, wherein said circuit is applied to a liquid crystal display (col. 4, lines 53-56).

It would have been obvious to one of ordinary skill in the art to use the circuit of Lei in a liquid crystal display as taught by Asma, due to the well-known slow response of liquid crystal displays which makes them especially susceptible to motion artifacts.

With respect to claim 21, Lei discloses, a first nonlinear quantizer (72 in fig. 4), for receiving a first frame data (input of 72 in fig. 4) and quantizing said first frame data by using a nonlinear quantization method to output said second frame data (output of 72; input of 76); and

a second nonlinear quantizer (66 in fig. 4), for receiving said third frame data (input of 72 in fig. 4) and quantizing said third frame data by using a nonlinear quantization method to output said fourth frame data (output of 72; input of 76);

a frame memory module (100 in fig. 4), coupled to said first nonlinear quantizer, receiving said second frame data and outputting a fifth frame data (output of 84) corresponding to said second frame data, said second frame data being shown in a motion picture after said fifth frame data (clear from fig. 4);

a signal converter (68, 70, 80 in fig. 4), for receiving said first frame data (output of 68 in fig. 4), said third frame data (input of 68 in fig. 4), said fourth frame data (top input of 80 in fig. 4) and said fifth frame data (right input of 80 in fig. 4) generate a

compensation data (output of 80 in fig. 4) and to output a sixth frame data (output of 68) and a seventh frame data (output of 80).

Lei does not expressly disclose, including data flow switchers in the circuit.

Van Asma discloses, a first data flow switcher (input line memory in fig. 4), for receiving a eighth frame data (first input into "lin mem" in fig. 4) and a ninth frame data (subsequent input into "lin mem" in fig. 4) and transforming said eighth frame data and ninth frame data to output the first frame data and the third frame data, said first data flow switcher outputs one of said first frame data and said third frame data (sequential outputs of "lin mem" in fig. 4); and

a second data flow switcher (DA in fig. 4), for receiving said sixth frame data and said seventh frame data and transforming said sixth frame data and seventh frame data to output a tenth frame data and a eleventh frame data, said second data flow switcher outputs one of said tenth frame data and said eleventh frame data (sequential outputs of DA in fig. 4).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the data flow switchers of Van Asma in the circuit of Lei.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

With respect to claim 22, Lei discloses, the circuit of claim 21 (see above), wherein said frame memory module comprises:

a frame memory (78 in fig. 4).

Lei does not expressly disclose including buffers and a multiplexer in the frame memory module.

Van Asma discloses, a circuit for simplifying display circuitry, comprising:

a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said second frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a fifth frame data (input of FIFO2), and first-in-first-out outputting said fifth frame data (output of FIFO2);

a frame memory, for storing a motion picture data (SDRAM in fig. 3); and

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory,

for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said fifth frame data from said frame memory to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace small frame memory of Lei with the frame buffer, containing a multiplexer unit and the dual port buffers, of Van Asma.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

With respect to claim 23, Lei and Van Asma disclose, the circuit of claim 22 (see above).

Lei further discloses, a motion picture enhancing unit (80 in fig. 4), for simultaneously receiving said fourth frame data and said fifth frame data and comparing said fourth frame data and said fifth frame data to generate said compensation data based on the difference between said fourth frame data and said fifth frame data (col. 1, lines 50-54; col. 6, lines 33-34); and

a first data processing unit (70 in fig. 4), for simultaneously receiving said first frame data and said compensation data corresponding to said twelfth frame data, and compensating said twelfth frame data based on said compensation data to obtain said fourth frame data (col. 6, lines 50-52)

a second data processing unit (68 in fig. 4), for simultaneously receiving said third frame data and said compensation data corresponding to said third frame data, and compensating said third frame data based on said compensation data to obtain said fifth frame data (col. 6, lines 50-52).

With respect to claim 24, Lei and Van Asma disclose, the circuit of claim 21 (see above).

Lei does not expressly disclose, wherein said circuit is applied to a liquid crystal display.

Van Asma further discloses, wherein said circuit is applied to a liquid crystal display (col. 4, lines 53-56).

It would have been obvious to one of ordinary skill in the art to use the circuit of Lei in a liquid crystal display as taught by Van Asma, due to the well-known slow response of liquid crystal displays which makes them especially susceptible to motion artifacts.

With respect to claims 25-30, Lei and Van Asma disclose, the circuit of claims 15-20 (see above). As claims 11-14 are merely method versions of these claims, they are rejected on the same merits shown above in the rejections of claims 15-20.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William L. Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

wlb
1/8/08

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